IP2183_D

Fast Charging Physical Layer IC for USB Interfaces

QC3.0/QC2.0,FCP,SCP,AFC,MTK PE+ 2.0/1.1,Apple 2.4A,BC1.2

1. Features

- Support 9 charging standards including :
  - QC3.0/QC2.0, AFC, SCP, FCP, MTK PE2.0/1.1
  - Apple 2.4A, Samsung 2.0A and BC1.2
- Support Qualcomm® QC3.0/QC2.0 Class A
  - QC3.0 Class A: 3.6V~12V(0.2V/step)
  - QC2.0 Class A: 5V, 9V, 12V
- MTK PE2.0/1.1
  - PE+ 2.0: 5V~20V(0.5V/step)
  - PE+ 1.1: 5V/7V/9V/12V
- Support Samsung® AFC
- Support Huawei® SCP
- Support Huawei® FCP
- Support Apple 2.4A: DP=2.7V, DM=2.7V
- Support Samsung 2.0A: DP=1.2V, DM=1.2V
- Support BC1.2: DP short DM automatically
- Default 5 V mode operation
- Support auto-detect and auto-switching fast charging standards
- FB for voltage regulation
- SEL configure the maximum voltage, allowed to applied for, as 20V or 12V or 5V
- Support DP,DM overvoltage protection
- Support DP,DM weak short to GND protection
- VIN working voltage: 3.3V~20V
- Package: SOP8

2. Description

IP2183 is a fast charging Physical Layer IC dedicated for USB ports, which supports 9 kinds of fast charging standards, including HVDCP QC2.0 /QC3.0 (Quick Charge), AFC (Samsung® Adaptive Fast Charge)，SCP (Hisilicon® Super Charge Protocol) and FCP (Hisilicon® Fast Charge Protocol), MTK PE+2.0/ PE+1.1(MediaTek Pump Express Plus 2.0/1.1), Apple 2.4A, BC1.2 and Samsung 2.0A.

IP2183 support automatically detecting the connected device's type and switching standards type to responding for fast charging requirements.

FB control line support sink or source current (2uA/step) for accurate voltage regulation.

3. Typical Applications

- USB power output ports for AC adapters, Power Banka, Car chargers
- Battery chargers for smart phones, tablets, netbooks, digital cameras, and Bluetooth accessories

4. Typical Application Schematic
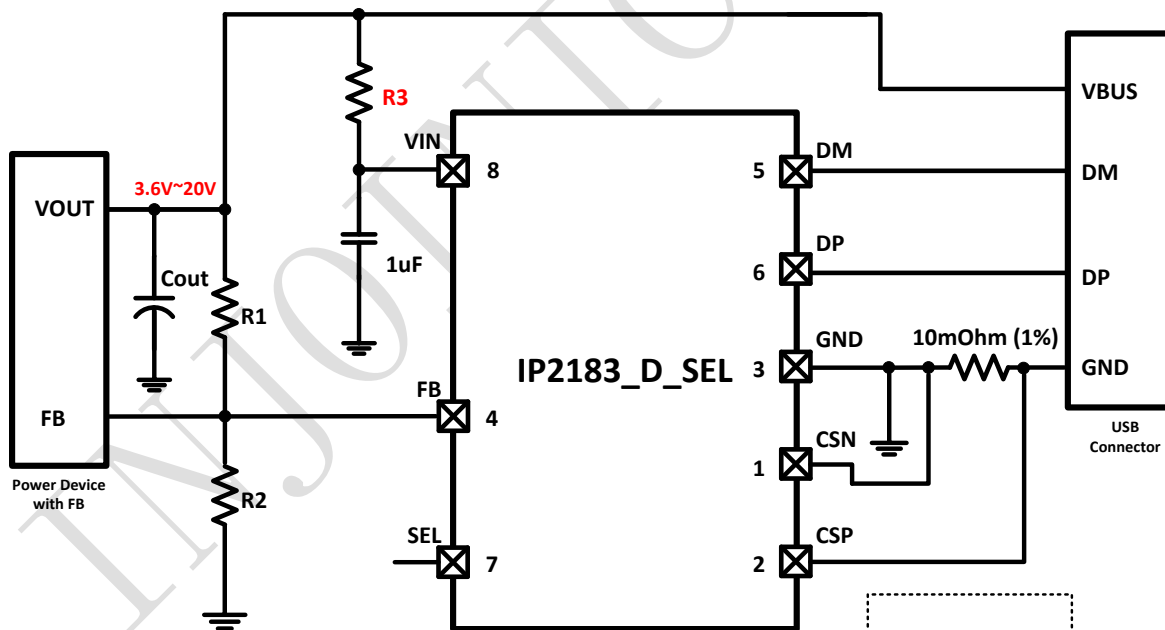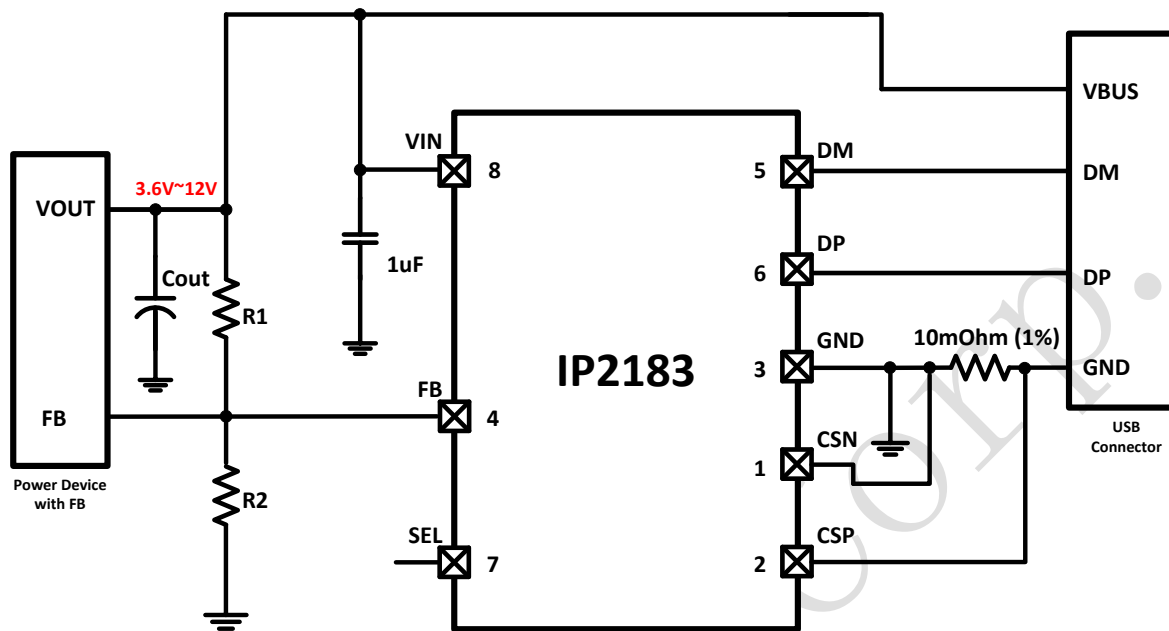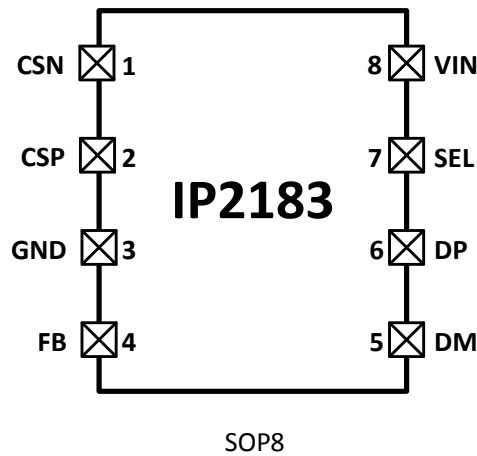

R1 Recommend: 100kOhm (1%)
R2 value refer to the power device
R3 value is 100ohm, as 20V application is needed

SEL	IP2183	IP2183_SEL
High	12V	5V
Float	12V	12V
GND	12V	20V

5. PIN Description

SOP8
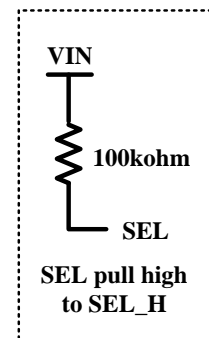
Pin No.	Pin Name	Description
1	CSN	Negative current sense node
2	CSP	Positive current sense node
3	GND	Ground
4	FB	Connect to the FB line of Regulator or opto-coupler, current source/sink for voltage regulation
5	DM	Connect to the DM pin of the USB port
6	DP	Connect to the DP pin of the USB port
7	SEL	Configure the maximum voltage allowed to apply for: • V SELH for 5V output • Floating for 12V output • GND for 20V output
8	VIN	Power Input

6. IP Series Products List

USB Charging Port Control IC

IC Part No.	Channel Num	Standard Supported											Package	
		BC1.2 & APPLE	QC3.0 & QC2.0	FCP	SCP	AFC	SFCP	MTK PE+ 2.0&1.1	Type C	NTC	QC Certificate	PD3.0	PKG	P2P
IP2110	1	√	-	-	-	-	-	-	-	-	-	-	SOT23-5	
IP2111 IP2111A	1	√	-	-	-	-	-	-	-	-	-	-	SOT23-6	
IP2112 IP2112A	2	√	-	-	-	-	-	-	-	-	-	-	SOT23-6	

IP2161	1	√	√	√	-	√	√	-	-	-	√	-	SOT23-6	
IP2163	1	√	√	√	-	√	√	√	-	√	√	-	SOP8	PIN2PIN
IP2183	1	√	√	√	√	√	-	√	-	-	-	-	SOP8	
IP2188	1	√	√	√	√	√	-	√	√	-	-	√	SSOP10	
IP2701	1	√	√	√	-	√	√	-	√	-	-	-	SOP8	
IP2703	1	√	√	√	-	√	√	√	√	√	-	-	DFN10	
IP2705	1	√	√	√	-	√	√	√	√	√	-	-	DFN12	
IP2707	2	√	√	√	-	√	√	√	√	√	-	-	QFN16	
IP2712	1	√	√	√	√	-	-	1.1	√	-	√	√	TSSOP20L	
IP2716	1	√	√	√	√	√	-	1.1	√	-	√	√	QFN32	
IP2723	1	√	√	√	√	√	-	√	√	-	-	√	TSSOP16	
IP2721	1	-	-	-	-	-	-	-	-	-	-	√ SINK	TSSOP16	

Power Bank IC

IC Part No.	Charge/Discharge		Features									Package	
	Charge	Discharge	LED Num	Lighting	Key	I2C	DCP	Type-C	QC Certificate	PD3.0/PPS	PKG	P2P
IP5303	1.0A	1.2A	1,2	√	√	-	-	-	-		eSOP8	PIN2PIN
IP5305	1.0A	1.2A	1,2,3,4	√	√	-	-	-	-		eSOP8	
IP5306	2.4A	2.1A	1,2,3,4	√	√	-	-	-	-		eSOP8	
IP5206	2A(Max)	1.5A	3,4,5	√	√	-	-	-	-		eSOP16	PIN2PIN
IP5108E	2.0A	1.0A	3,4,5	√	√	-	-	-	-		eSOP16	
IP5108	2.0A	2.0A	3,4,5	√	√	√	-	-	-		eSOP16	
IP5207	1.2A	1.2A	3,4,5	√	√	-	-	-	-		QFN24	PIN2PIN
IP5207T	1.2A	1.2A	1,2,3,4	√	√	√	√	-	-		QFN24	
IP5109	2.1A	2.1A	3,4,5	√	√	√	-	-	-		QFN24	
IP5209	2.4A	2.1A	3,4,5	√	√	√	√	-	-		QFN24	
IP5219	2.4A	2.1A	1,2,3,4	√	√	√	√	√	-		QFN24	
IP5310	3.1A	3.0A	1,2,3,4	√	√	√	√	√	-		QFN32	
IP5312	15W	3.6A	2,3,4,5	√	√	√	√	-	-		QFN32	
IP5318Q	18W	4.0A	2,3,4,5	√	√	√	√	-	√		QFN40	PIN2PIN
IP5318	18W	4.0A	2,3,4,5	√	√	√	√	√	√		QFN40	
IP5322	18W	4.0A	1,2,3,4	√	√	√	√	-	√		QFN32	
IP5328	18W	4.0A	1,2,3,4	√	√	√	√	√	√		QFN40	PIN2PIN
IP5328P	18W	4.0A	1,2,3,4	√	√	√	√	√	√		QFN40	

　　Copyright © 2017, Injoinic Corp.

7. Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
VCC Input Voltage Range	VIN	-0.3 ~ 30	**V**
DP, DM Input Voltage Range	V_{DP}, V_{DM}	-0.3~15	**V**
Other Pins Input Voltage Range	V_{other}	-0.3~10	**V**
Junction Temperature Range	T_J	-40 ~ 150	℃
Storage Temperature Range	T_{STG}	-60 ~ 150	℃
Lead Temperature Range (Soldering, 10sec)	T_s	260	℃
Package Thermal Resistance	θ_{JA}	90	℃
Package Thermal Resistance	θ_{JC}	39	℃
Human Body Model (HBM)	ESD	2	**KV**

*Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

*Voltages are referenced to GND unless otherwise noted.

8. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Voltage	VIN	3		25	V
Ambient Temperature	T_A	-40		85	℃

*Devices' performance cannot be guaranteed when working beyond those Recommended Operating Conditions.

9. Electrical Characteristics

Unless otherwise specified, T A =25℃, 4.5V ≤ VCC ≤ 5.5V

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Voltage	VIN	Supplied directly	3		25	V
Input UVLO Threshold	UVLO	VIN Falling	2.5		2.9	V
Quiescent Current	I_Q	No load, VIN=5V	1			mA
		No load, VIN=20V			1.6	mA
Startup Time	Ts		20	37	50	us
HVDCP (QC2.0&QC3.0)						
Data Detect Voltage Threshold	V_{DATA_REF}		0.25	0.325	0.4	V

Output Voltage Selection Reference	V_{SEL_REF}		1.8	2	2.2	V
DP High Glitch Filter Time	$T_{GLITCH(BC)\_DP\_H}$		1000	1250	1500	ms
DM Low Glitch Filter Time	$T_{GLITCH(BC)\_DM\_L}$			2		ms
Output Voltage Glitch Filter Time	$T_{GLITCH(V)\_CHANGE}$		20	40	60	ms
Continuous Mode Glitch Filter Time	$T_{GLITCH\_CONT\_CHANGE}$		100		200	us
DM Pull-down Resistance	R_{DM_DOWN}	VDP=0.6V		20		kOhm
DP Pull-down Resistance	R_{DAT_LKG}	VDP=0.6V		500		kOhm
FB Current Step	I_{UP}, I_{DOWN}	40uA(9V); 70uA(12V); 150uA(20V)		2		uA
DCP						
Samsung DP/DM Output Voltage			1.08	1.2	1.32	V
Samsung DP/DM Output Impedance				100		kOhm
Apple 2.4A DP/DM Output Voltage			2.64	2.7	2.76	V
Apple 2.4A DP/DM Output Impedance				30		kOhm

10. Function Description

Charging Standards

IP2183 is a high-voltage, fast charging Physical Layer IC dedicated for charging applications where charging standards required to be negotiated between USB ports. IP2183 is needed at the host-side, when the attached portable client-side device negotiate the power allotment from the power source host-side, IP2183 can auto-detect and respond to the those charging standards and may grant or deny the request based on the available voltage/current. IP2183 will inform the power source host-side to adjust the output voltage by FB line once charging request granted.

IP2183 support analysis several charging standards, including HVDCP QC3.0 (Quick Charge), AFC (Adaptive Fast Charge), SCP (Super Charge Protocol) and FCP (Fast Charge Protocol).

IP2183 detects both CC pins for USB PD protocol and monitors the real-time voltage on DP line and DM line for other fast charge protocol detection. Once the attached device fast charge type is determined, the negotiation will be accomplished on CC lines or DP and DM lines accordingly. IP2183 will analysis the protocol and fulfill the

power requirements, source/sink current on FB line to grant the request voltage. When the output voltage is default 5V, FB line neither source nor sink current.

IP2183 is not in control of the charging power loop, the actual charging loop and charging current is determined by the host-side power source and the client-side USB port device.

SEL

SEL line is used to configure the maximum voltage allotment that can be request, when SEL line is pull up to high-voltage of V SELH , the IP2183_SEL will not respond to any fast charging requirements and output default 5V; When SEL line is floating, IP2183_SEL the maximum voltage allotment is 12V; When SEL line is pull down to GND, IP2183_SEL the maximum voltage allotment is 20V.

*Note: SEL pull 100kohm resistor to VIN is V SELH .

SEL	IP2183	IP2183_SEL
High(V$_{SELH}$)		5V
Float	12V	12V
GND		20V

*Note: when the typical application schematic option 2 is adopted, SEL used for selecting the maximum voltage function is disabled.

FB

IP2183 integrated FB control line used for accurate voltage regulation by source/sink current with precise 2uA/step in minimum. FB sink 40uA current for 9V output voltage; FB sink 70uA current for 12V output voltage; FB sink 150uA current for 20V output voltage; when the output voltage is default 5V, FB neither source nor sink current.

In typical applications, IP2183 FB connects to the regulator's FB line, resistor (R1) between VOUT and FB should apply 100kOhm with high precision (1%), resistor (R2) value between FB and GND should refer to the regulator adopted, resistance of R2 can be calculated by equation:

$$VFB = \frac{VOUT}{R1+R2} * R2$$

11. Package
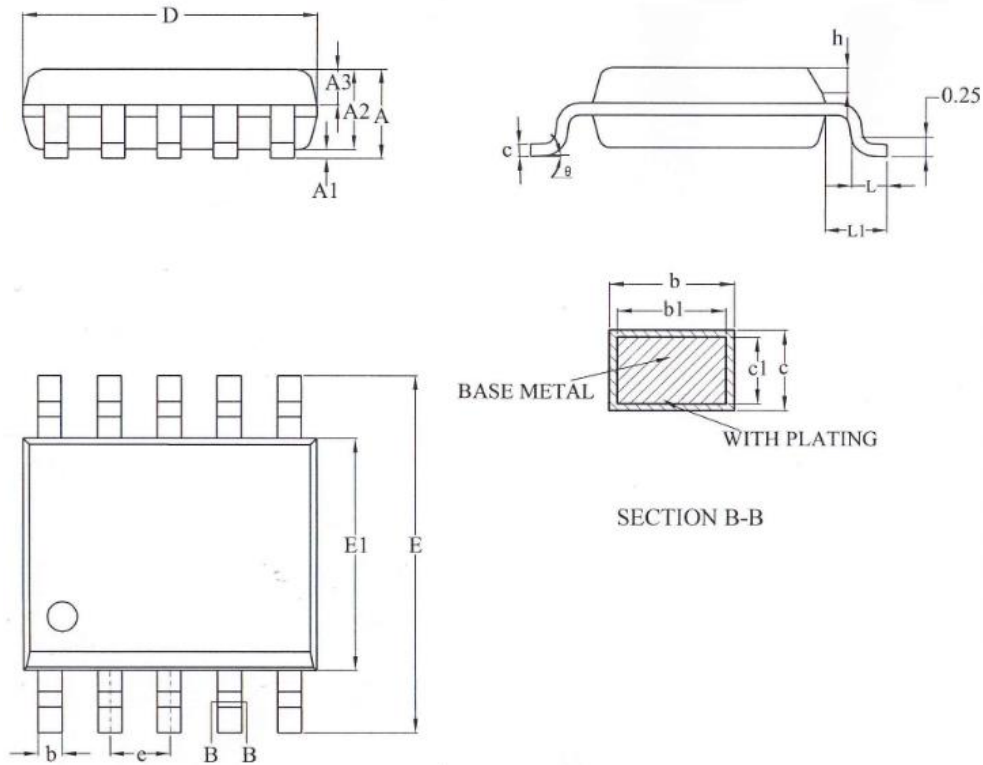
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.00BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

BASE METAL

WITH PLATING

SECTION B-B

12. IMPORTANT NOTICE

INJOINIC TECHNOLOGY and its subsidiaries reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to INJOINIC TECHNOLOGY's terms and conditions of sale supplied at the time of order acknowledgment.

INJOINIC TECHNOLOGY assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using INJOINIC TECHNOLOGY's components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of INJOINIC TECHNOLOGY's components in its applications, notwithstanding any applications-related information or support that may be provided by INJOINIC TECHNOLOGY. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify INJOINIC TECHNOLOGY and its representatives against any damages arising out of the use of any INJOINIC TECHNOLOGY's components in safety-critical applications.

Reproduction of significant portions of INJOINIC TECHNOLOGY's information in INJOINIC TECHNOLOGY's data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. INJOINIC TECHNOLOGY is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

INJOINIC TECHNOLOGY will update this document from time to time. The actual parameters of the product may vary due to different models or other items. This document voids all express and any implied warranties.

Resale of INJOINIC TECHNOLOGY's components or services with statements different from or beyond the parameters stated by INJOINIC TECHNOLOGY for that component or service voids all express and any implied warranties for the associated INJOINIC TECHNOLOGY's component or service and is an unfair and deceptive business practice. INJOINIC TECHNOLOGY is not responsible or liable for any such statements.